Robust and Performing RF LDMOS Device Integrated in a VLSI BCD Silicon Technology

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Abstract — **A high performance RF LDMOS device suitable for RF power amplifier handsets applications has been successfully integrated in a 0.35 μm pure silicon BCD technology. In this paper, device architecture, DC, small signal and load pull performances are shown, together with device model description and accuracy.**

I. INTRODUCTION

Compound semiconductor (GaAs, InGaP, GaN, etc.) devices are commonly used for RF power applications because of their high cutoff frequency, breakdown voltage, power density and efficiency. Anyway, many efforts in development of silicon LDMOS as well as lithography scaling down, allowed the use of this pure silicon device for power amplifiers at frequencies up to 2 GHz [1]-[2]. Previous RF LDMOS power amplifiers (PA) products were not compatible with standard VLSI CMOS technologies and discrete solutions have been used. Recently, the integration of a RF LDMOS in 0.25 μm SiGe:C BICMOS process has been reported, with the advantage of CMOS high integration level capability [3]. In this work, we present the integration of a high performance RF LDMOS device in a pure silicon VLSI BCD technology. This process platform allows lower cost, better device engineering and all the advantages of a VLSI CMOS technology. Process features, RF LDMOS performances and device modeling accuracy are also presented.

II. TECHNOLOGY DESCRIPTION

In a pure silicon VLSI BCD technology power LDMOS device performances are maximized, maintaining at the same time the fully compatibility with the CMOS and non volatile memories platform of the same VLSI lithography generation. In particular, BCD6 is a 0.35 μm technology based on 3.3V CMOS platform built on p^-/p^+ substrate with twin retrograde wells, high energy implanted triple well for isolated pockets, double flavored gates, self aligned silicide technique, W plugs, five metal levels and CMP planarized intermetal dielectrics [4].

The BCD6 high modularity in term of number of masks and process options allows a simplified and optimized version of the technology, named RF-BCD6, for low cost high performance power amplifiers suitable for 3G cellular phones. In RF-BCD6 technology a large device library is available, comprehensive of 16 V RF LDMOS, 3.3 V and 5 V CMOS, 20 V *n* and *p*-channel drift MOS, 5 V NPN, 20 V LPNP, low and high resistance poly resistors, high linear MIM capacitors and thick Al:Cu metal inductors.

III. RF LDMOS ARCHITECTURE

In RF-BCD6 technology, RF LDMOS device has been integrated optimizing performances and reliability at the same time. In Fig. 1 device cross-section is shown. The substrate is an already epitaxied p^- on p^+ wafer used in standard VLSI CMOS technology for high ruggedness against latch-up. The DMOS source side is realized with large tilt angle implantation: angle, dose and energy have been carefully optimized in order to have short channel length, low leakage current, low threshold voltage but not short channel effects. n^+ source and p^+ body contacts are shorted thanks to the self-aligned silicidation technique. This method allows a low source series resistance as well as a uniform and efficient grounding of the body, avoiding premature turn on of the intrinsic parasitic NPN. The p^- on p^+ substrate allows the use of high dose implanted p^+ sinkers to have low resistive paths for source current from top to bottom of the chip. This feature let the cumbersome and inductive source wire bondings be avoided. Only 7nm gate oxide has been used to drive the gate with 3.3 V but maintaining high transconductance while drain design has been optimized to have low on-state resistance and high breakdown voltage at the same time. Output characteristics of the optimized RF LDMOS are shown in Fig. 3 for a 50 μm width device.

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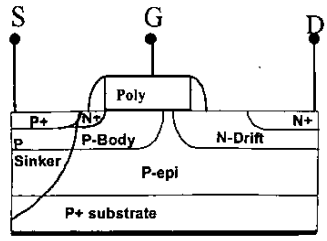


Fig. 1. BCD6 RF LDMOS cross section.

IV. RF LDMOS ELECTRICAL PERFORMANCES

The main DC and small signal AC performances of BCD6 RF LDMOS are shown in Table I.

The specific (per unit source width) on-state resistance (*Ron* = 2.8 Ωmm), high BV_{DSS} and high transconductance, together with high F_T, make RF LDMOS a device suitable for high efficiency 2 GHz cellular phones power amplifiers operating at 3.5 V battery voltage. The best data reported previously have shown similar BV_{DSS} and F_T but worst on state resistance, transconductance and current capability at about the same power supply [2]-[3].

TABLE I
MAIN ELECTRICAL PARAMETERS

Parameter	Value	Test Condition
BV_{DSS} [V]	16	I_{DS} = 0.01 nA/μm
I_{OFF} [pA/μm]	<1	V_{DS} = 5 V V_{GS} = 0
*Ron*W* [Ω*mm]	2.8	V_{GS} = 3.3 V V_{DS} = 0.1 V
Gm/W [mS/mm]	200	V_{DS} = 3.5 V
I_{SAT}/W [mA/mm]	480	V_{DS} = 3.5 V
F_T [GHz]	18	V_{DS} = 3.5 V

Load-pull measurements have been performed to evaluate RF saturated and linear power performances.

Single tone measurements on RF LDMOS single stages have shown 73 % power added efficiency (PAE) at 0.9 GHz and 65 % at 2 GHz with an output power level of about 24.3 dBm and 25.8 dBm, respectively (see Fig. 4 and 5). These performances make the device very competitive for GSM/DCS/PCS PA standards. WCDMA load-pull measurements have been performed, showing that, being the carrier 2 GHz, an adjacent channel power ratio (ACPR) of –38 dBc can be guaranteed, achieving a PAE = 44 % (Fig. 10 and 11). This high linearity and efficiency makes the device suitable for WCDMA 3G PA application too. These good performances were obtained using only 3.5V bias.

The intrinsic device robustness has been observed after an extreme load mismatch, VSWR = 10:1 @ *Vcc* = 5 V, in GSM and DCS modes. A further confirmation has been obtained from the hot carriers sensitivity, which is one of the main causes of RF LDMOS failure in standard PA. In fact results of preliminary reliability are very satisfactory. A single stage 2 GHz PA, made by a RF LDMOS with *W* = 2.8 mm, mounted on a FR4 PCB has been monitored for a week, with the double of standard bias 3.5 V, with a Pin settled at 3dB power compression. As represented in Fig. 2, each of three DUTs has a negligible degradation, showing a good reliability against hot carriers even at high power levels.

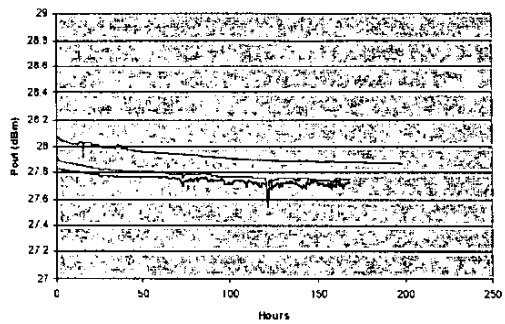


Fig. 2. Output power @3dB compression point as function of stress time

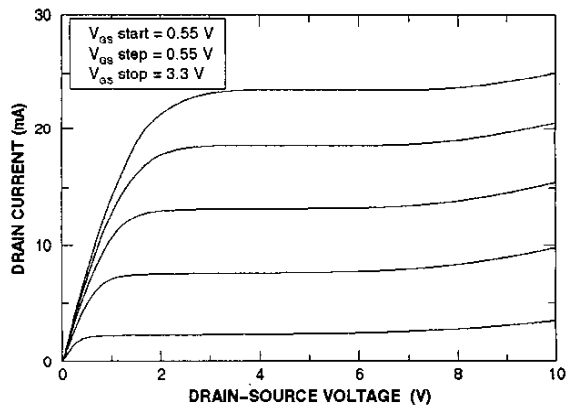


Fig. 3. BCD6 RF LDMOS output characteristics.

V. RF DMOS MODEL DESCRIPTION AND ACCURANCY

RF DMOS device has been modeled through the circuit shown in Fig. 6.

The intrinsic MOS is simulated by University of Berkeley BSIM3 model. The use of the latest version

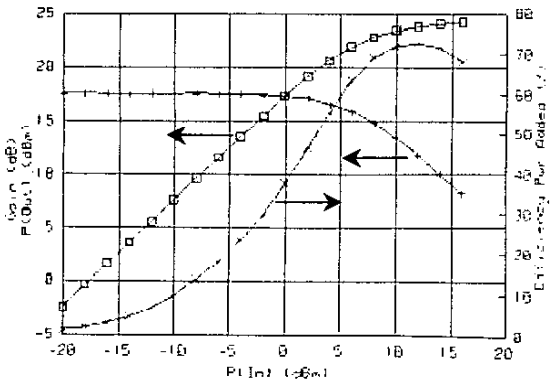
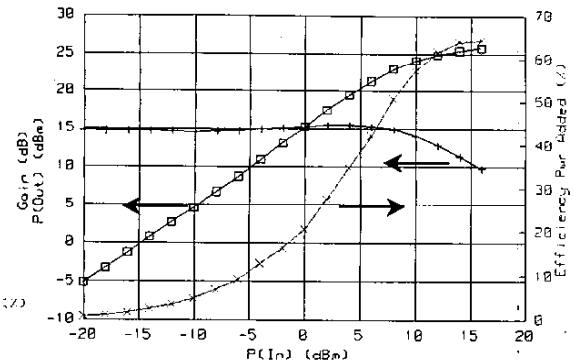


Fig. 4. Output power, gain and power added efficiency @f = 0.9 GHz.



allows the increasing of the accuracy of the gate capacitance and in weak inversion through extra parameters available also in BSIM4 model. The gate-source and gate-drain extrinsic capacitances have been included in BSIM model adopted for the intrinsic MOS. The drain drift region is modeled by a non linear resistor (GRDEPI) which takes into account the modulation of the conductance of *n*-body layer under the gate oxide. The resistors R_S and R_D describe the contribution of contacts and metals to source and drain series resistances, respectively. R_{Ge} takes into account the extrinsic gate resistance due to the gate poly and metal. The diode D_{BDL} models the *n*-body/*p*-body+p^- junction while the parasitic metal capacitance is described by C_{DS}.

Several complex scaling rules have been introduced to properly reproduce the electrical behavior of devices of various sizes and geometries with *W* ranging from 20 µm to 20 mm. The model has been successfully implemented both for ELDO RF [5] and ADS [6] simulators.

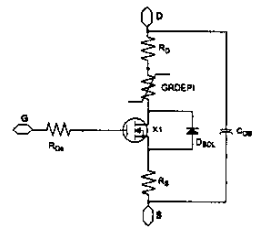


Fig. 6. RF LDMOS subcircuit.

The model accuracy is illustrated in Fig. 7-11, where the circuit simulations are compared to the experimental data obtained in DC, AC and large RF signal conditions. In particular excellent results have been achieved in the simulation of gm and gate capacitances. An accurate evaluation of the gate/drain capacitance that is strongly non-linear is usually regarded as an issue in the modeling.

Another critical point is the proper simulation of first and second order derivatives of *gm* that is mandatory for an evaluation of RF PA linearity performances (intermodulation products for ACPR). Both goals have been achieved by the model extracted for RF LDMOS.

Excellent agreement between experimental data and simulations has been obtained also in the standard RF large signal measurements tested by the load-pull technique.

An important parameter for WCDMA power amplifier is the ACPR which value could limit the maximum PA efficiency. The model presented allows a reliable simulation of ACPR for RF LDMOS.

VI. Conclusion

A high performance and robust RF LDMOS device has been successfully integrated in a mature 0.35 µm BCD process. RF LDMOS device characteristics and related models have been demonstrated to be suitable for high efficiency GSM/DCS and WCDMA handsets PA stages realization. Furthermore, the large device library availability and the possible easy migration to smaller lithography BCD processes makes RF VLSI BDC a real low cost silicon solution for high integrated RF power systems.

Acknowledgement

We want to thank all the involved people from ACCO-USA for their contribution to load pull measurements and useful discussions for technology and modeling optimization.

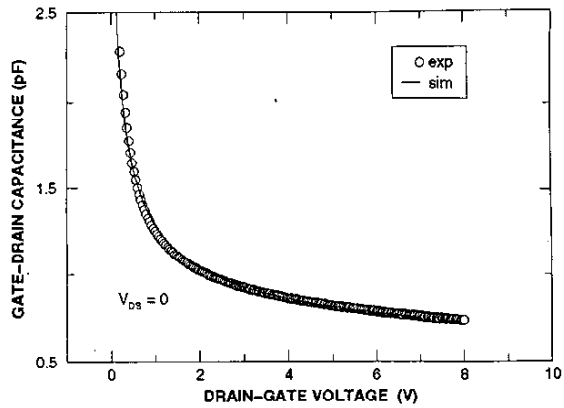


Fig. 7. C_{GS}: experimental and simulated data.

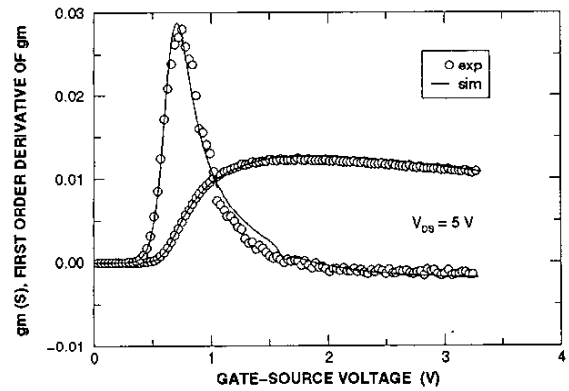


Fig. 8. *gm* and its first order derivative: exp. and sim. data.

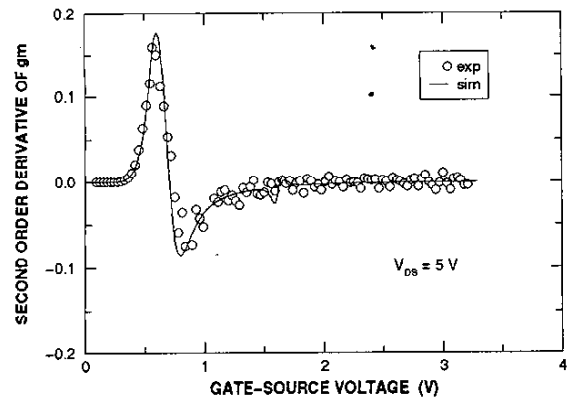


Fig. 9. Second derivative of *gm*: exp. and sim. data.

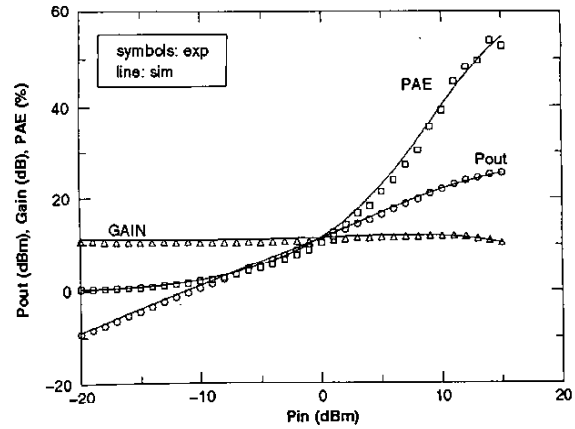


Fig. 10. Output power, gain and power added efficiency for 2GHz WCDMA standard: experimental and simulated data.

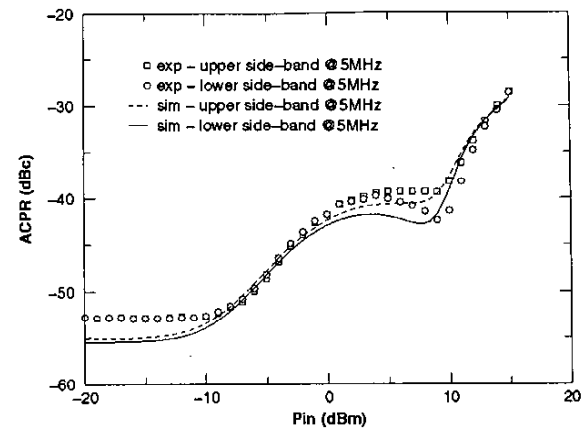


Fig. 11. Adjacent channel power ratio, upper and lower side-band @ 5MHz: experimental and simulated data.

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